and the pulse duration measuring circuit 175 to the pulse duration measuring means, respectively.

When a high voltage pulse is not generated, the output of the high voltage pulse detecting circuit 83 becomes high level and is then inputted to the AND gate 69. The output voltage of the armature winding 3 having passed the high frequency noise filter circuit 64 (voltage appearing at the output terminal of the alternator 1) is applied to the negative terminal of the voltage comparator 65, in which the regulated voltage Vreg is applied to the positive terminal. When this input voltage is lower than the regulated voltage Vreg, the output becomes high level. When this input voltage is higher than the regulated voltage Vreg, the output becomes low level and is then inputted to the AND gate 69.

The high(Hi)/low(Lo) conditions of the output of the voltage comparator 65 are applied to the transistor drive circuit 85 from the AND gate 69. The power transistor 61 is turned on and off by the transistor drive circuit 85. Thereby, the output voltage of the alternator 1 is adjusted to the predetermined value Vreg (for example, 14.5V).

Next, operations when a high voltage pulse is generated will be explained.

Fig. 10 is a timing diagram illustrating the signal waveforms inputted or outputted to or from each section of the voltage regulator 6 of this embodiment in the case where one high voltage pulse is generated.

When a comparatively large electric load is cut off, one

high voltage pulse is generated on the power supply line 8. Since the peak value of this high voltage pulse is higher than the regulated voltage Vreg, an output of the voltage comparator 65 becomes low level and the power transistor 61 is quickly turned off. Thereafter, when a voltage pulse that is higher than the breakdown voltage of the full-wave rectifier 4 formed of the power Zener diode is applied, the power Zener diode reaches the breakdown point to absorb the energy of the high voltage pulse. In order to detect the high voltage pulse, the reference voltage V3, that is higher than the regulated voltage Vreg and is lower than the breakdown voltage is set.

When the voltage of the power supply line 8 is higher than this reference voltage V3, the output of the voltage comparator 66 within the high voltage pulse detecting section 160 becomes high level. With a rising edge of this output signal, operation of the timer circuit 171 within the discriminating section 170 is triggered. While the timer circuit 171 is operating, the AND gate 172 outputs directly the output signal of the voltage comparator 66. The pulse counting circuit 173 is structured to maintain an output of low level for the single pulse input and provide an output of high level for two or more pulse inputs.

Therefore, when a high voltage pulse is generated once in the power supply line 8, the output of the pulse counting circuit 173 becomes low level and output of the AND gate 174 also becomes low level. In this timing, the pulse duration measuring circuit 175, timer circuit 181 and output control circuit 182 do not operate, and the output of the output control circuit 182 is

maintained at high level. Thereafter, the peak value of the high voltage pulse is lowered and the output voltage of the alternator 1 is adjusted to the regulated voltage Vreg.

Next, operation when a high voltage pulse is generated frequently will be explained below. Fig. 11 is a timing diagram illustrating signal waveforms inputted or outputted to or from each section of the voltage regulator 6 of this embodiment when a high voltage pulse is generated frequently.

If a connection failure occurs on the power supply line 8, a high voltage pulse is generated frequently on the power supply line 8. While the voltage applied to the high voltage pulse detecting circuit 83 is higher than the reference voltage V3, the output of the voltage comparator 66 is in the high level. With a rising edge of this output signal, operation of the timer circuit 171 is triggered. The timer circuit 171 operates whenever the output of the voltage comparator 66 rises and while a high voltage pulse is generated frequently, the output voltage becomes high level. Therefore, the AND gate 172 passes the output signal of the voltage comparator 66 to the pulse counting circuit 173, while the high voltage pulse is generated frequently and the output of the timer circuit 171 is at the high level.

When the high voltage pulse is repeatedly applied, the pulse counting circuit 173 provides an output of high level at the second rising edge of output of the AND gate 172. This high level condition of output is maintained until a reset pulse (k) is inputted from the timer circuit 181 to the pulse counting circuit 173 and the pulse duration measuring circuit 175.